

**CLAIMS**

What is claimed is:

Sub AI

1. An apparatus comprising:
  - a task table coupled to a bus interface to store task entries corresponding to tasks executed by at least one processor;
  - a block allocation circuit coupled to the bus interface and a cache memory to allocate blocks of the cache memory used by at least one of the tasks; and
  - a task coordinator to coordinate the tasks in response to a task cycle issued by the at least one processor.
2. The apparatus of claim 1 wherein each of the task entries comprises at least one of a task status, a task identifier (ID), a task start address, a task block size, and a task cache address.
3. The apparatus of claim 2 wherein the task cycle provides at least one of a task ID, a task command, the task start address, and the task block size.
4. The apparatus of claim 3 wherein the block allocation circuit comprises:

2                   a search logic circuit to locate a free block by shifting through a list of  
3                   busy flags corresponding to data blocks in use in the cache memory; and

4                   a block information generator coupled to the block search logic to  
5                   generate block information of a free block available for a new task, the block  
6                   information including at least a block size, a block starting address, and a block  
7                   ending address.

1               5. The apparatus of claim 1 wherein the task coordinator comprises:

2                   a task table updater to update the task table; and

3                   an address generator to generate address information to the cache  
4                   memory.

1               6. The apparatus of claim 3 wherein the task status is one of an invalid  
2                   status, a shared status, and an exclusive status.

1               7. The apparatus of claim 6 wherein the task command is one of a read  
2                   shared command, a read exclusive command, a write command, and a flush command.

1               8. The apparatus of claim 7 wherein the task block size corresponds to  
2                   number of cache lines in one of the blocks.

1           9.     The apparatus of claim 8 wherein the bus interface is one of a processor  
2     bus interface and a multiprocessor bus interface.

1           10.    The apparatus of claim 9 wherein the cache memory is one of an internal  
2     cache and an external cache with respect to the at least one processor.

1           11.    A method comprising:  
2                   storing task entries corresponding to tasks executed by at least one  
3     processor in a task table;  
4                   allocating blocks of the cache memory used by at least one of the tasks;  
5     and  
6                   coordinating the tasks in response to a task cycle issued by the at least  
7     one processor.

1           12.    The method of claim 11 wherein each of the task entries comprises at  
2     least one of a task status, a task identifier (ID), a task start address, a task block size,  
3     and a task cache address.

1           13.    The method of claim 12 wherein the task cycle provides at least one of  
2     the task ID, a task command, the task start address, and the task block size.

1        14. The method of claim 13 wherein allocating comprises:

2                locating a free block by shifting through a list of busy flags

3                corresponding to data blocks in use in the cache memory; and

4                generating block information of a free block available for a new task, the

5                block information including at least a block size, a block starting address, and a

6                block ending address.

1        15. The method of claim 11 wherein coordinating the tasks comprises:

2                updating the task table; and

3                generating address information to the cache memory.

1        16. The method of claim 13 wherein the task status is one of an invalid

2        status, a shared status, and an exclusive status.

1        17. The method of claim 16 wherein the task command is one of a read

2        shared command, a read exclusive command, a write command, and a flush command.

1        18. The method of claim 17 wherein the task block size corresponds to

2        number of cache lines in one of the blocks.

1           19. The method of claim 18 wherein the bus interface is one of a processor  
2       bus interface and a multiprocessor bus interface.

1           20. The method of claim 19 wherein the cache memory is one of an internal  
2       cache and an external cache with respect to the at least one processor.

1           21. A system comprising:  
2           a processor bus; and  
3           a plurality of processors coupled to the processor bus, each of the  
4       plurality of processors having an internal task manager and an internal cache  
5       memory, the internal task manager comprising:  
6           a task table coupled to a bus interface to store task entries  
7       corresponding to tasks executed by at least one processor,  
8           a block allocation circuit coupled to an internal bus interface and  
9       the interval cache memory to allocate blocks of the interval cache  
10      memory used by at least one of the tasks, and  
11           a task coordinator to coordinate the tasks in response to a task  
12      cycle issued by the at least one processor.

1           22. The system of claim 21 wherein each of the task entries comprises at  
2           least one of a task status, a task identifier (ID), a task start address, a task block size,  
3           and a task cache address.

1           23. The system of claim 22 wherein the task cycle provides at least one of  
2           the task ID, a task command, the task start address, and the task block size.

1           24. The system of claim 23 wherein the block allocation circuit comprises:  
2                   a search logic circuit to locate a free block by shifting through a list of  
3                   busy flags corresponding to data blocks in use in the internal cache memory;  
4                   and  
5                   a block information generator coupled to the block search logic to  
6                   generate block information of a free block available for a new task, the block  
7                   information including at least a block size, a block starting address, and a block  
8                   ending address.

1           25. The system of claim 21 wherein the task manager comprises:  
2                   a task table updater to update the task table; and  
3                   an address generator to generate address information to the interval  
4                   cache memory.

1           26. The system of claim 23 wherein the task status is one of an invalid  
2       status, a shared status, and an exclusive status.

1           27. The system of claim 26 wherein the task command is one of a read  
2       shared command, a read exclusive command, a write command, and a flush command.

1           28. The system of claim 27 wherein the task block size corresponds to  
2       number of cache lines in one of the blocks.

1           29. The system of claim 28 wherein the processor bus is a multiprocessor  
2       bus.

1           30. The system of claim 9 further comprising:  
2       a external cache memory; and  
3       an external task manager coupled to the external cache memory and the  
4       processor bus, the external task manager comprising:  
5               an external task table to store task entries corresponding to tasks  
6       executed by at least one processor,

7 a external block allocation circuit coupled to the processor bus  
8 and the external cache memory to allocate blocks of the external cache  
9 memory used by the tasks, and  
10 an external task coordinator to coordinate the tasks in response to  
11 the task cycle issued by the at least one processor.